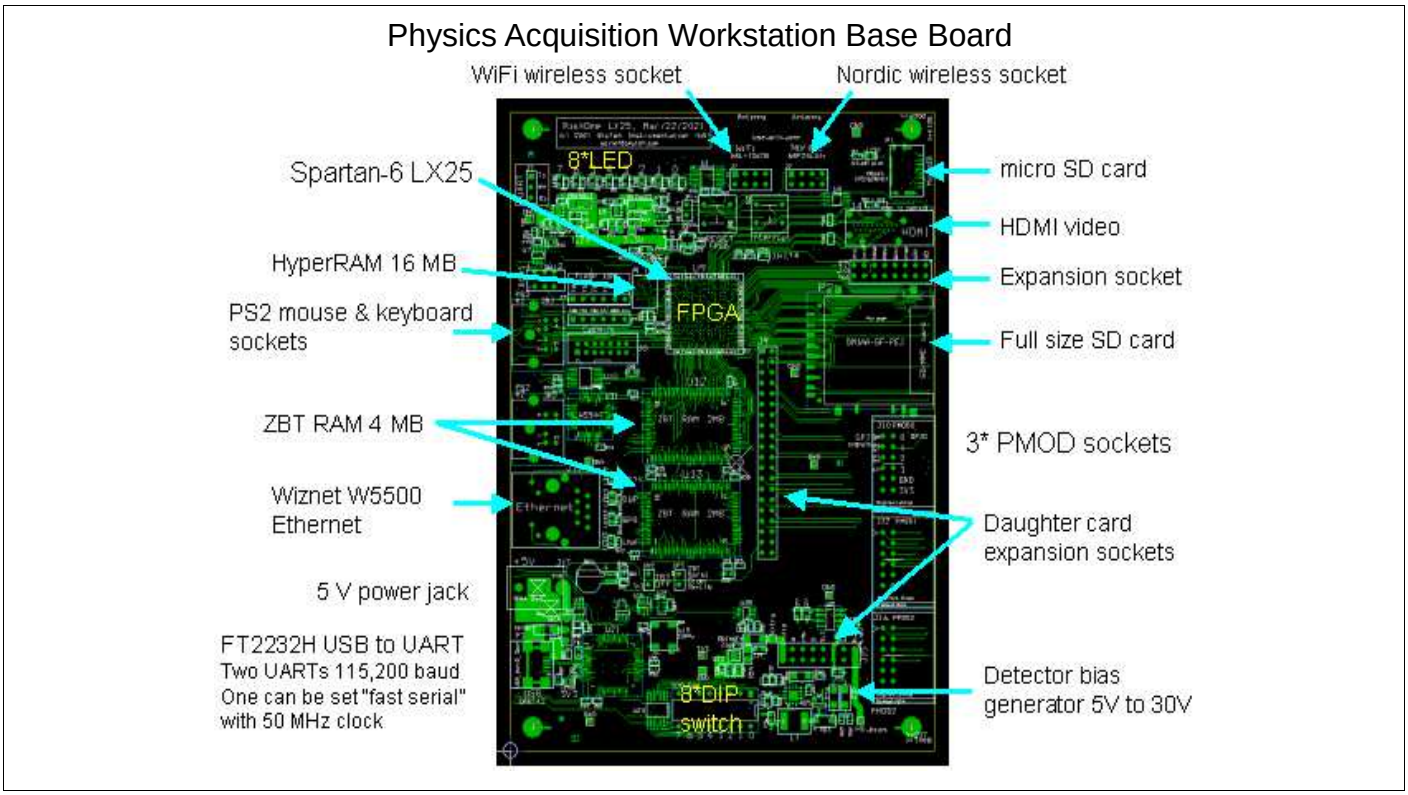

PAWS Jr. is a compact, low cost Base Board for entry level instruments and data acquistion system. It uses ORTOS software for control and data processing, running on a processor core embedded in an entry level Spartan-6 LX25 Field Programmable Gate Array (FPGA). Ample memory is available for the operating system, applications, and data. Three 0.1" expansion connectors enable the user to develop application extensions, utilizing standard prototyping boards with 0.1" perforation. Advanced users can develop their own daughter PCBs using standard EDA tools such as OrCAD, KiCAD, or Eagle. Three PMOD-compatible connectors enable using low cost PMOD modules, such as ADC, DAC, OLED displays, keypads, or remote signal drivers. Detector bias generator programmable in the range +5V to +30V will be ideal for biasing silicon photomultiplers, PIN diodes, and other similar particle or optical detectors.

- LX25 FPGA specifications.
- PAWS Jr. can be assembled with LX9, LX16, or LX25. The latter is recommended.
- If using the LX25: 30,064 flip flops, 38 multiply-accumulate DSP slices, 52 BRAM blocks (18 Kb each).

- Expansion socket specifications.
- 0.1" pin sockets arranged in the standard 0.1" grid will allow using standard pre-perforated prototyping boards.
- All signals are driven with 3.3V LVCMOS levels, or other standards supported by the FPGA at Vcc=3.3V.
- I2C, SPI, FPGA reset (the DONE signal) and two GPIOs available on the North expansion socket.
- Thirty-two FPGA GPIO pins available on the West expansion socket (the large vertical one in the Figure).
- +5V, -5V, +3.3V, +1.8V, and +5V to +30V detector bias available on the South expansion socket.

- Digital PMOD-compatible connector specifications.
- Three PMOD connectors according to Digilent PMOD specification, each with eight signals and 3.3V power.
- The North PMOD has all eight signals individually routed to the FPGA. (Not shared with any other connector.)
- The Middle and the South PMODs share the SPI and four GPIO pins with other subsystems.

- Memory specifications.
- 104 kilobytes of fully embedded Block RAM (BRAM), assuming that parity bits are not used.
- Four MB of fast Zero Bus Turnaround (ZBT) memory running up to 200 MHz * 32 bits.
- Sixteen MB (one chip) of dynamic HyperRAM with on-chip refresh controller, running up to 100 MHz.

- USB to serial interface specifications.
- One FT2232H chip , converting the USB-2 interface to two independent UARTs connected to the FPGA.
- One UART running at one of the standard baud rates up to 115,200 baud.
- The 2nd UART can be configured as a "serial optical link" with the clock running up to 50 MHz.
- An additional 3-pin connector which can be configured as an optional UART independent from the above.

- On-board mass storage.
- One micro SD card socket wired as the SPI device, sharing a board wide SPI bus with the other SPI devices.
- One full size SD card socket, with all signals individually routed to the FPGA (not shared).

- Ethernet specifications.
- One Wiznet W5500 SPI-to-Ethernet controller with the on-chip TCP/IP stack, using the board wide SPI bus.

- Wireless specifications.
- One 8-pin connector wired for the Nordic NRF24L01 packet radio module, connected to board-wide SPI.
- One 8-pin connector wired for the WiFi plugin module Sparkfun WRL-13678, wired directly to the FPGA.

- Hardware User interfaces.
- Two PS2 connectors for a PS2 mouse and a PS2 keyboard.
- One full size HDMI connector for an external monitor.

- Embedded soft processor core and peripherals.
- 32-bit RISC5 soft processor core with the Instruction Set Architecture (ISA) optimized for running ORTOS.
- 32-bit bus internal to the FPGA for accessing on-chip peripherals (SPI, I2C, video frame buffer, etc.).
- Optional floating point support.
- Deterministic interrupt activation after three CPU clock cycles.
- Open source Verilog implementation of a very small size.

- Free open source ORTOS software development and operating system provided with the instrument.
- Free and open source ORTOS GUI with the resident editor and the compiler running directly on board.
- Run time model implementing the "terminate and stay resident" (TSR) architecture.
- Strongly typed Oberon programming language with garbage collection for memory management.

- Supported by commercial Astrobe software development and operating system.
- The commercial Astrobe GUI for cross-compilation of ORTOS software using a Windows PC.
- Astrobe ORTOS is available from CFBsoftware.com. Contact the Astrobe vendor to obtain a license.

- Compatibility with other FPGAs or microprocessors.
- Originally ORTOS was developed with the Spartan-3 Starter Kit, using Spartan-3 XC3S200.
- ORTOS was then ported to Spartan-6 LX9, LX45, various Artix-7, and Spartan-7 devices.
- Full ORTOS with graphics and resident compilation chain runs in several emulated environments.
- Astrobe ORTOS is also supporting the ARM Cortex-M processors. See CFBsoftware.com for details.

- **Advantages.**
- Low cost FPGA for hosting the customer's firmware, the soft core, and standard peripherals.
- Predictable and deterministic real time response to interrupts.
- Software development using a high level language. Neither an assembler nor low level C are required.
- Signal post processing can be performed by the RISC5 soft core augmenting the FPGA firmware. In most cases, developing ORTOS software will be significantly easier than developing the FPGA firmware.

Please send an e-mail to info@skutek.com for more information.